ECE 385  
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Lab 4

Simple Computer SLC-3.2 in SystemVerilog

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**Introduction**

**Pre-Lab Question**

**.SV Modules**

**Module**: Processor.sv

**Inputs**: Clk, Reset\_Load\_Clear, Run, [9:0] SW

**Outputs**: [6:0] HEX(0-6), [7:0] Aval, [7:0] Bval, Xval

**Description**: This module is the top level of this circuit and is used to instantiate all the modules within it. This includes the control unit, mux, registers, the adder, and the hex drivers.

**Purpose**: This module takes the input signals from the FPGA, directs the signals to perform the necessary operations, and displays the outputting signals on the hex displays. This is displayed in the top-level diagram above.

**State Diagram for Control Unit**

**Annotated Simulation Waveforms  
Post-Lab**

1. **Design Statistics Table**

|  |  |
| --- | --- |
| LUT | 113 |
| DSP | 0 |
| Memory(B-Ram) | 0 |
| Flip-Flop | 21 |
| Frequency | 50 Mhz |
| Static Power | 89.94 mW |
| Dynamic Power | 0.00 mW |
| Total Power | 98.73 mW |

1. **Post-Lab Questions**

**Conclusion**